Amendments to the Specification:

In the SUMMARY OF THE INVENTION,
please replace the 1st full paragraph on page 5 with the following amended paragraph:

In the same way as described in the referenced patent application (US Serial No. 10/764920), within a set of small capacitors, one capacitor after the other is switched in parallel to change the total sum of capacitance. To achieve a linear capacitance change, said capacitors are not switched on one by one in digital steps, however each capacitor is switched on partially in a sliding operation, starting at low value (0 % of its capacitance) and ending with the fully switched on capacitor (100 % of its capacitance) , i.e. the capacitor is switched on with increasing (or decreasing) share. To achieve said sliding switch operation, a typical implementation uses FET- type transistors as switching device, one per capacitor. The switching operation of such FET-type transistor can be divided into three phases: the fully-switched-off phase (said FET transistor's drain-source-resistance RDS is very high), a steady ramp-up/ramp-down phase or steady transition phase (that is: said FET transistor's resistance RDS is changing between very high resistance and very low resistance in a linear and steady mode) and the fully-switched-on phase (said FET transistor's drain-source-resistance RDS is very low). By thoroughly controlling such switching device within said linear and steady ramp-up/ramp-down phase, the capacitor in series with said switching device is partially switched in parallel with a well-controlled proportion between 0 % and 100 %.

In the BRIEF DESCRIPTION OF THE DRAWINGS add and replace the following:

Fig. 10b shows a circuit added to modify the reference voltage for temperature compensation.

Fig. 10~~b~~c shows ~~the~~ an added circuit to generate a temperature compensated reference voltage.

In the DESCRIPTION OF THE PREFERRED EMBODIMENTS, please replace the 1st full paragraph starting at page 18 with the following amended paragraph:

In the same way as described in said related patent application US Serial No. 10/764920, within a set of small capacitors **Cap 1** to **Cap n**, one capacitor after the other is switched in parallel to change the total capacity. Each capacitor has its individual switching device **Sw 1** to **Sw n.** To achieve a linear capacitance change, said capacitors are not switched on one by one in digital steps, however each capacitor is switched on partially in a sliding operation, starting at low value (0 % of its capacitance) and ending with the fully switched on capacitor (100 % of its capacitance), i.e. the capacitor is switched on with increasing (or decreasing) share. To achieve said sliding switch operation, a typical implementation uses FET- type transistors, one per capacitor. The switching operation of such FET-transistor can be divided into three phases: the fully-switched-off phase (the FET transistor's drain-source-resistance RDS is very high), a steady ramp-up/ramp-down phase or steady transition phase, where the series resistance of said FET-transistor linearly follows the gate voltage and steadily changes from high to low values or vice versa, and the fully-switched-on phase (said FET transistor's drain-source-resistance RDS is very low). **Fig. 10b** in US Patent Application Serial No. 10/764920, included by reference, visualizes the principal RDSon characteristic versus gate voltage of the switching devices **N1-5** of a single capacitor

switching stage according to **Fig. 5** of the present application. By thoroughly controlling such switching device within said steady ramp-up/ramp-down or steady transition area, the capacitor in series with said switching device is effectively switched in parallel to the other capacitors with a well-controlled proportion between 0 % and 100 %. "Steady" is meant in the mathematical sense of being free of jumps or breaks. The limits of said steady ramp-up/ramp-down or steady transition area is distinguished by the points, where a further change of the controlling signal of the switch does not lead to further decrease or increase of the series resistance of said switching device (except for a small, negligible change).

Please replace the 1st full paragraph starting at page 23 with the following amended paragraph:

Similar to the input reference levels in **Fig. 9**, the output reference levels could be provided for example through a resistor network to provide individual output reference levels for each translinear amplifier (**Ref-out-1** to **Ref-out-n**). Another possible and a minimal solution, ~~to~~ provideing ~~the~~ an identical output reference level to all translinear amplifiers, could be to connect ~~a single signal to~~ all output reference points of all translinear amplifiers (equivalent to **Ref-out-1** to **Ref-out-n** in **Fig. 6**) to a common output reference level **C-Ref-out**, as it is shown in **Fig. 9**.

Please replace the last[t] paragraph starting at page 28 and extending to page 29 with the following two pragraphs:with the following amended paragraph:

Furthermore, a concept of this disclosure is to compensate the temperature deviation, caused by the temperature characteristics of the switching device; **Fig. 10b** presents this concept, which shows a temperature compensating circuit **Temp-Comp** in addition to said circuit to control the switching operation **Switch-Ctrl**, as shown in **Fig.**

5. One method is to use a device **N2-10** of the identical type of the switching device **N1-10** to produce a temperature dependent signal. A temperature compensating voltage, produced by said device **N2-10**, is added to the output reference signal **Ref-out-10**, now resulting in a temperature compensated output reference signal **Ref-out-c-10.** The input of said temperature compensating circuit **Temp-Comp** is connected to the reference circuit **RefCirc** of **Fig. 6** and its output ~~and feed it as compensating voltage **Vref-10**~~ is then provided ~~in~~to the output reference point **Voutn-10** of the translinear amplifier. This compensation technique will mirror the exact equivalent of the temperature error into the switching control signal **Vg-~~10~~** and compensate its temperature error. The output reference point **Voutn-10** in **Fig. 10b** is the same point as the reference signals **Ref-out** in **Fig. 5**.

As already described with **Fig. 9**, a simplified solution providing an identical output reference level to all translinear amplifiers could be to connect a common signal to all output reference points **Ref-out** (equivalent to **Voutn** of the translinear amplifiers) in common. In the case of providing an identical temperature compensated reference voltage as a common signal, it would be sufficient to implement a single temperature compensating circuit to serve all said output reference points **Ref-out** in common. **Fig. 10c** presents such simplified and common temperature compensating circuit.